



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,382	04/22/2004	Tomoyasu Nakamine	TSUT.0030	7090
7590	08/04/2005		EXAMINER BERRY, RENEE R	
Stanley P. Fisher Reed Smith Suite 1400 3110 Fairview Park Drive Falls Church, VA 22042-0681			ART UNIT	PAPER NUMBER
			2818	
DATE MAILED: 08/04/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/829,382	<b>Applicant(s)</b> NAKAMINE ET AL.	
	<b>Examiner</b> Renee R. Berry	<b>Art Unit</b> 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |  |
|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/22/04</u> . | 6) <input type="checkbox"/> Other: ____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,495,054 to Eguchi et al. in view of US Patent No. 5,994,678 to Zhao et al.

In regards to claim 1, Eguchi teaches a semiconductor device manufacturing method using a film forming apparatus having a film forming chamber for performing a film forming process to a semiconductor substrate, the film forming apparatus performing said film forming process at a first temperature, and including a step of forming a first thin film over said semiconductor substrate, the method comprising the steps of: (b) after said step (a), forming a plasma from a gas containing a halogen system gas, and removing an accretion attached in said film forming chamber by using said plasma (column 17, lines 17-23); and (c) after said step (b), cleaning an interior of said film forming chamber in a step of raising the interior of said film forming chamber up to said first temperature, wherein said film forming apparatus has, in said film forming chamber, a first member reacting with a halogen system element and generating a by-product (column 17, lines 37-60), and the method further comprises the step of: forming a second thin film on an inner wall of said film forming apparatus and on a surface of a member provided in said film forming chamber at the same temperature

Art Unit: 2818

as that after said accretion is removed in said step (b) or at a temperature before the interior of said film forming chamber reaches said first temperature in said step (c) (column 15, lines 31-38).

In regards to claim 2, Eguchi teaches the semiconductor device manufacturing method according to claim 1, wherein said first member contains a metal element or silicon at column 7, lines 1-5.

In regards to claim 5, Eguchi teaches the semiconductor device manufacturing method according to claim 1, wherein said first and second thin films contain silicon at column 9, lines 10-16 (BST and silicon oxide).

In regards to claim 6, Eguchi teaches the semiconductor device manufacturing method according to claim 5, wherein said second thin film includes a thin film of the same type as that of said first thin film at column 7, lines 1-25.

In regards to claim 7, Eguchi teaches the semiconductor device manufacturing method according to claim 1, wherein said film forming apparatus performs the film forming process by a chemical film forming method at column 6, lines 46-50.

In regards to claim 9, Eguchi teaches a film forming method using a film forming apparatus having a film forming chamber for performing a film forming process to a

Art Unit: 2818

substrate, the film forming apparatus performing said film forming process at a first temperature, and forming a thin film over said substrate, the method comprising the steps of: (b) after said step (a), forming a plasma from a gas containing a halogen system gas, and removing an accretion attached in said film forming chamber by said plasma (column 17, lines 17-23); and (c) after said step (b), cleaning an interior of said film forming chamber in a step of raising the interior of said film forming chamber up to said first temperature, wherein said film forming apparatus has, in said film forming chamber, a first member reacting with a halogen system element and generating a by-product (column 17, lines 37-60), and the method further comprises the step of: forming a second thin film on an inner wall of said film forming apparatus and on a surface of a member provided in said film forming chamber at the same temperature as that after said accretion is removed in said step (b) or at a temperature before the interior of said film forming chamber reaches said first temperature in said step (c) (column 15, lines 31-38).

In regards to claim 10, Eguchi teaches the film forming method according to claim 9, wherein said first member contains a metal element or silicon at column 7, lines 1-5.

In regards to claim 13, Eguchi teaches the film forming method according to claim 9, wherein said film forming apparatus performs the film forming process by a chemical film forming method at column 6, lines 46-50.

However, Eguchi does not teach all the limitations of the following claims:

In regards to claims 1 and 9, Zhao teaches after forming said first thin film over a predetermined number of said substrates, (a) decreasing a temperature in said film forming chamber up to a second temperature lower than said first temperature at column 35, lines 35-42 and column 40, lines 37-40.

In regards to claim 3, Zhao teaches the semiconductor device manufacturing method according to claim 1, wherein said first temperature is 600.degree C or higher, and said second temperature is a temperature at which no reaction of said halogen system element and said first element occurs at column 35, lines 35-42 and column 40, lines 37-40.

In regards to claim 4, Zhao teaches the semiconductor device manufacturing method according to claim 3, wherein said second temperature is 500 degree C or lower at column 40, lines 37-40.

In regards to claim 8, Zhao teaches the semiconductor device manufacturing method according to claim 1, wherein said semiconductor substrate has a diameter of 300 mm or larger at column 39, lines 30-32.

In regards to claim 11, Zhao teaches the film forming method according to claim 9, wherein said first temperature is 600 degree C or higher, and said second temperature

Art Unit: 2818

is a temperature at which no reaction of said halogen system element and said first element occurs at column 35, lines 35-42 and column 40, lines 37-40.

In regards to claim 12, Zhao teaches the film forming method according to claim 11, wherein said second temperature is 500 degree C or lower at column 40, lines 37-40.

In regards to claim 14, Zhao teaches the film forming method according to claim 9, wherein said semiconductor substrate has a diameter of 300 mm or larger at column 39, lines 30-32.


Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified Eguchi to include after forming said first thin film over a predetermined number of said substrates, (a) decreasing a temperature in said film forming chamber up to a second temperature lower than said first temperature, since such a modification would result in less chamber cleaning and higher substrate output, as described in column 5, lines 14-18 of Zhao et al.

**NOTE:** Gases possess the same ability to clean in plasma form and in gaseous form (PECVD or CVD).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R. Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
RRB  
April 16, 2005

  
David Nelms  
Supervisory Patent Examiner  
Technology Center 2800